FIG. 1

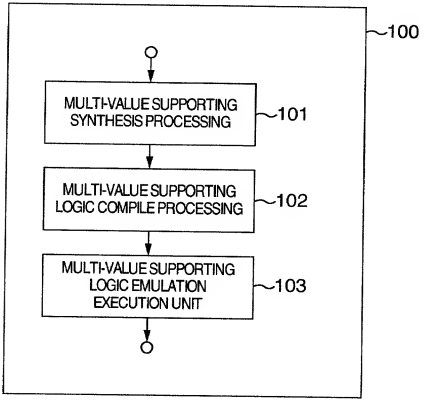

100
MULTI-VALUE SUPPORTING SYNTHESIS PROCESSING
101
MULTI-VALUE SUPPORTING LOGIC COMPILE PROCESSING
102
MULTI-VALUE SUPPORTING LOGIC EMULATION EXECUTION UNIT
103

FIG. 2

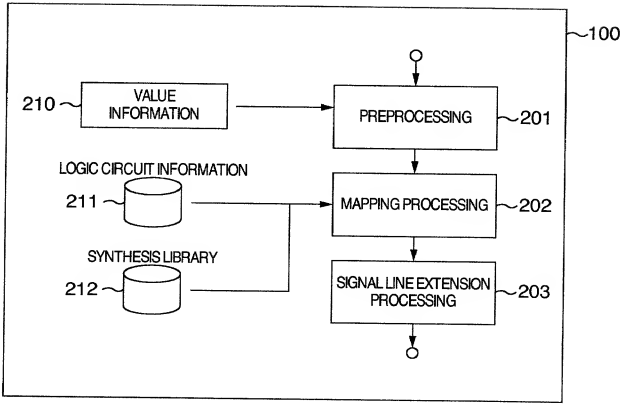
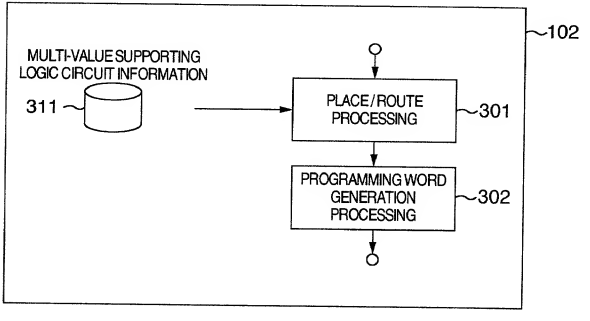

100
210
VALUE INFORMATION
PREPROCESSING
201
LOGIC CIRCUIT INFORMATION
211
MAPPING PROCESSING
202
SYNTHESIS LIBRARY
212
SIGNAL LINE EXTENSION PROCESSING
203

FIG. 3


102
MULTI-VALUE SUPPORTING LOGIC CIRCUIT INFORMATION
311
PLACE / ROUTE PROCESSING
301
PROGRAMMING WORD GENERATION PROCESSING
302

TOSHIBA 6596760

FIG. 4

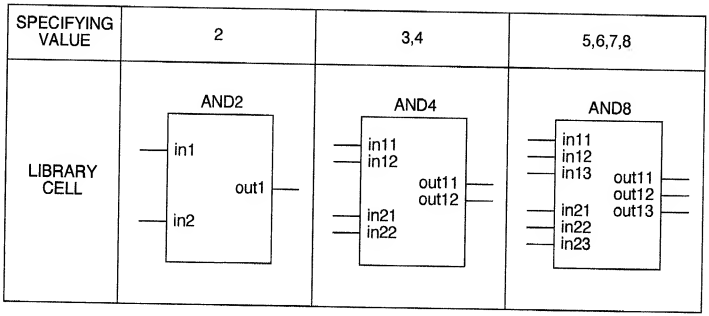


FIG. 5

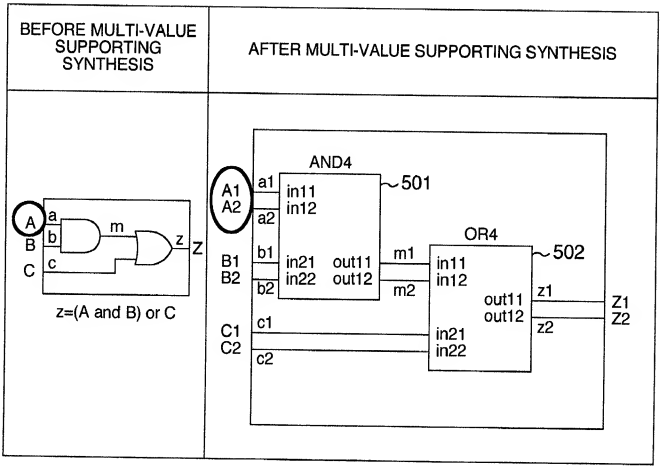

BEFORE MULTI-VALUE SUPPORTING SYNTHESIS
AFTER MULTI-VALUE SUPPORTING SYNTHESIS
A
B
C
a
b
c
m
z
Z
z=(A and B) or C
AND4
501
A1
A2
a1
a2
in11
in12
B1
B2
b1
b2
in21
in22
out11
out12
m1
m2
OR4
502
in11
in12
in21
in22
out11
out12
z1
z2
Z1
Z2
C1
C2
c1
c2

FIG. 6

600

601 LOGIC SIGNAL	602 PHYSICAL SIGNAL	603 TYPE	604 ATTRIBUTE
A	A1,A2	PORT	IN
B	B1,B2	PORT	IN
C	C1,C2	PORT	IN
Z	Z1,Z2	PORT	OUT
a	a1,a2	INTERNAL	——
b	b1,b2	INTERNAL	——
c	c1,c2	INTERNAL	——
z	z1,z2	INTERNAL	——
m	m1,m2	INTERNAL	——

FIG. 7

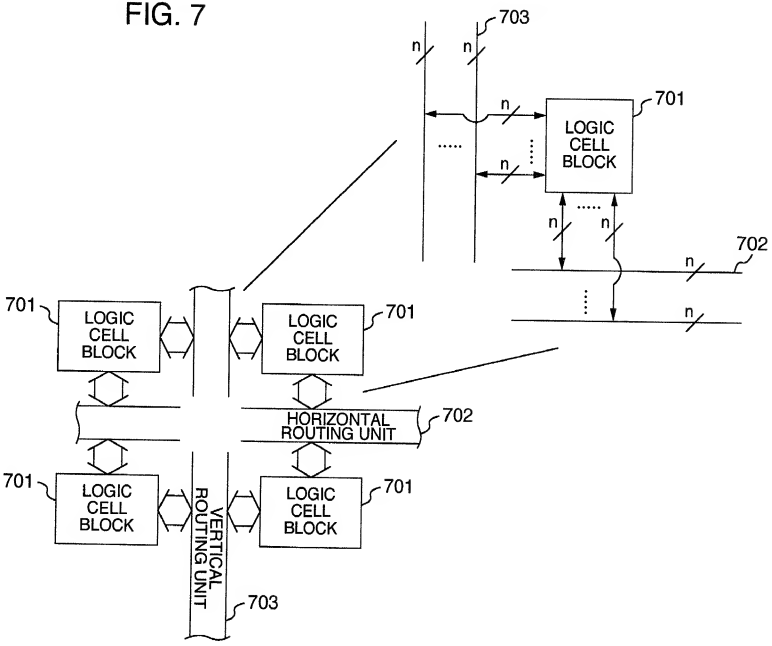

703
n
n
n
n
701
LOGIC CELL BLOCK
.....
n
n
.....
n
n
702
n
n
701
LOGIC CELL BLOCK
701
LOGIC CELL BLOCK
HORIZONTAL ROUTING UNIT
702
701
LOGIC CELL BLOCK
701
LOGIC CELL BLOCK
VERTICAL ROUTING UNIT
703

FIG. 8

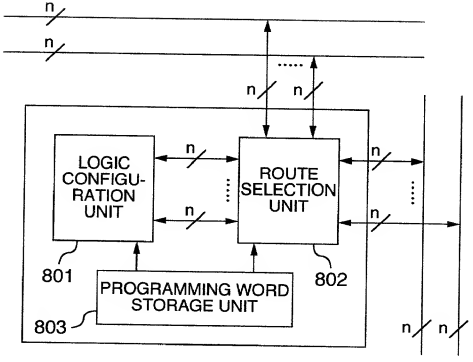
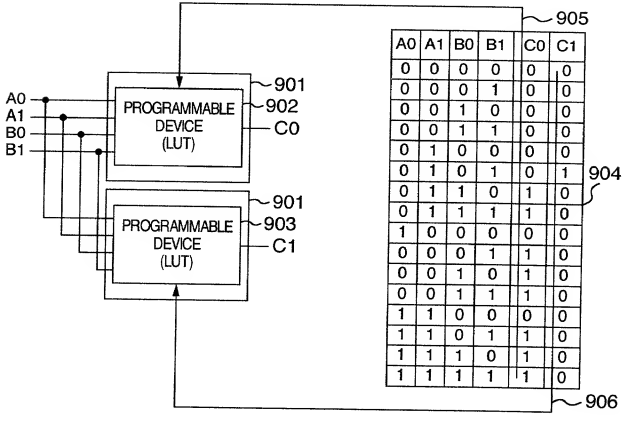
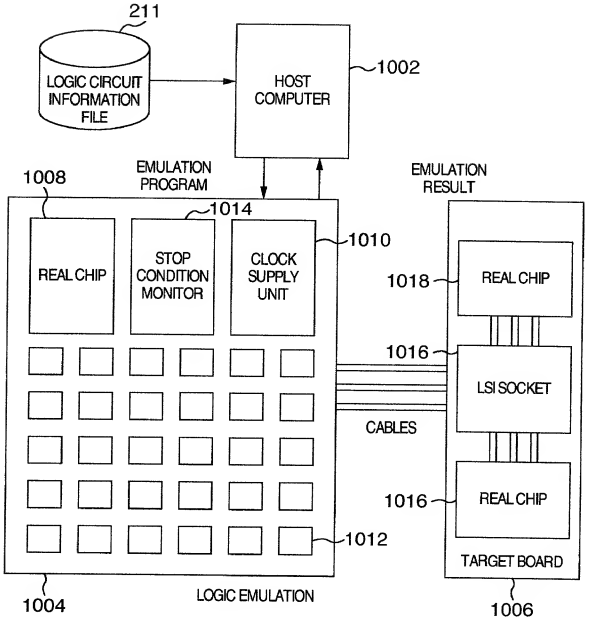


FIG. 9



A0	A1	B0	B1	C0	C1
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	0

FIG. 10


211
LOGIC CIRCUIT INFORMATION FILE
HOST COMPUTER
1002
1008
EMULATION PROGRAM
EMULATION RESULT
1014
REAL CHIP
STOP CONDITION MONITOR
CLOCK SUPPLY UNIT
1010
1018
REAL CHIP
1016
LSI SOCKET
CABLES
1016
REAL CHIP
1012
TARGET BOARD
1004
LOGIC EMULATION
1006